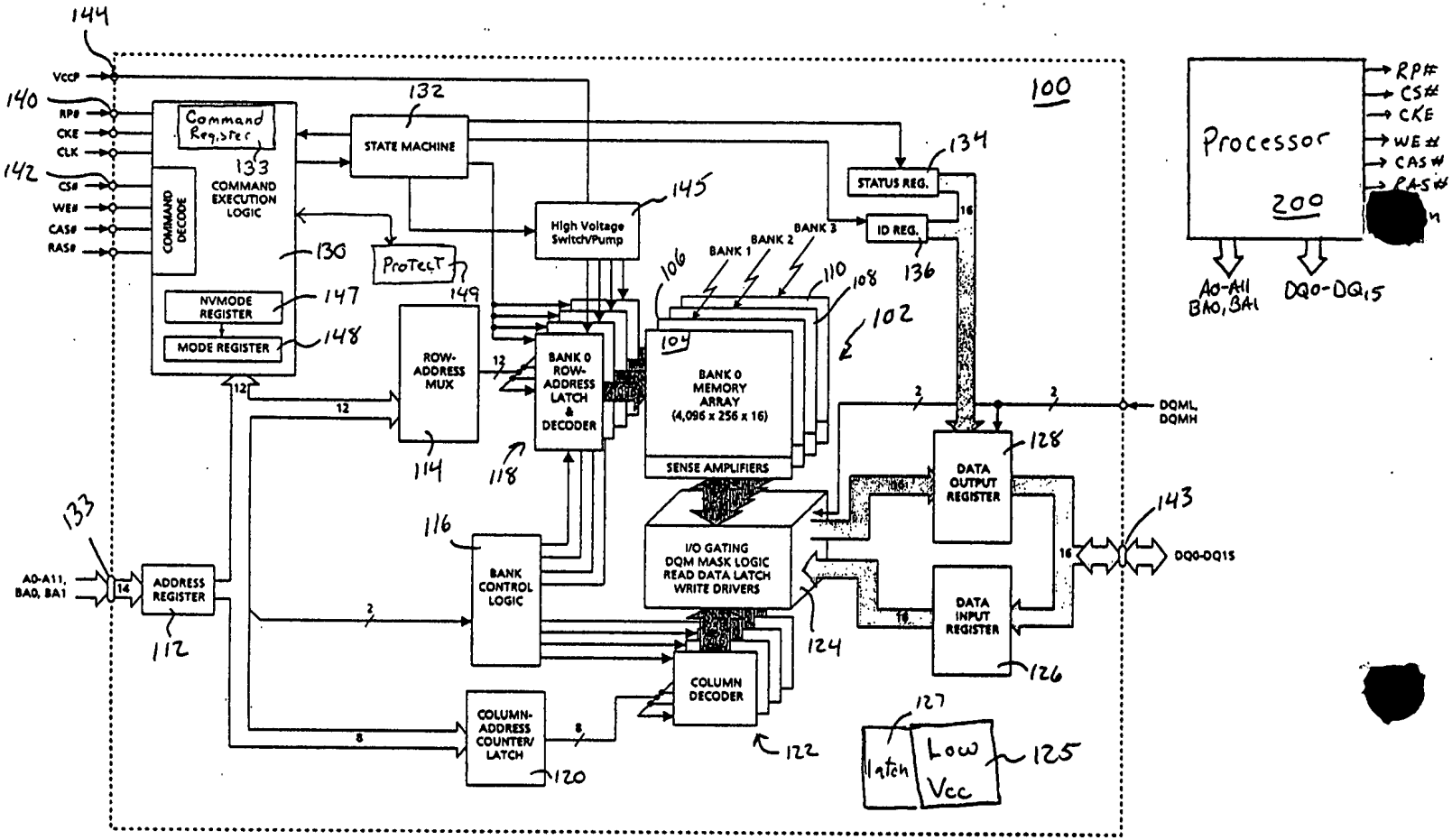

100
144
VCCP
140
RP#
CKE
CLK
142
CS#
WE#
CAS#
RAS#
Command Register
133
COMMAND EXECUTION LOGIC
COMMAND DECODE
132
STATE MACHINE
130
Protect
149
NVMODE REGISTER
147
MODE REGISTER
148
High Voltage Switch/Pump
145
STATUS REG.
134
ID REG.
136
BANK 0
BANK 1
BANK 2
BANK 3
106
110
108
104
102
ROW-ADDRESS MUX
114
BANK 0 ROW-ADDRESS LATCH & DECODER
118
BANK 0 MEMORY ARRAY (4,096 x 256 x 16)
SENSE AMPLIFIERS
DQML, DQMH
128
DATA OUTPUT REGISTER
143
DQ0-DQ15
133
A0-A11, BA0, BA1
ADDRESS REGISTER
112
116
BANK CONTROL LOGIC
I/O GATING DQM MASK LOGIC READ DATA LATCH WRITE DRIVERS
124
DATA INPUT REGISTER
126
COLUMN DECODER
122
COLUMN-ADDRESS COUNTER/ LATCH
120
127
latch
Low Vcc
125
Processor
200
RP#
CS#
CKE
WE#
CAS#
RAS#
A0-A11 BA0, BA1
DQ0-DQ15

Fig. 1A

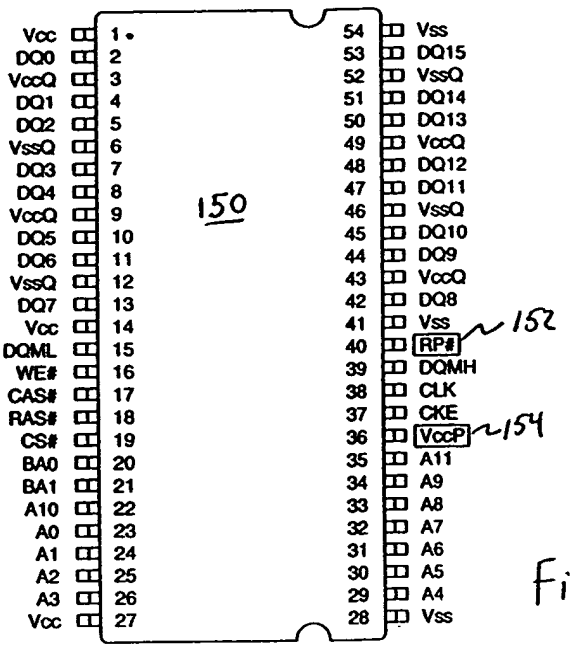

Vcc 1
DQ0 2
VccQ 3
DQ1 4
DQ2 5
VssQ 6
DQ3 7
DQ4 8
VccQ 9
DQ5 10
DQ6 11
VssQ 12
DQ7 13
Vcc 14
DQML 15
WE# 16
CAS# 17
RAS# 18
CS# 19
BA0 20
BA1 21
A10 22
A0 23
A1 24
A2 25
A3 26
Vcc 27
54 Vss
53 DQ15
52 VssQ
51 DQ14
50 DQ13
49 VccQ
48 DQ12
47 DQ11
46 VssQ
45 DQ10
44 DQ9
43 VccQ
42 DQ8
41 Vss
40 RP#
39 DQMH
38 CLK
37 CKE
36 VccP
35 A11
34 A9
33 A8
32 A7
31 A6
30 A5
29 A4
28 Vss
150
152
154

Fig. 1B

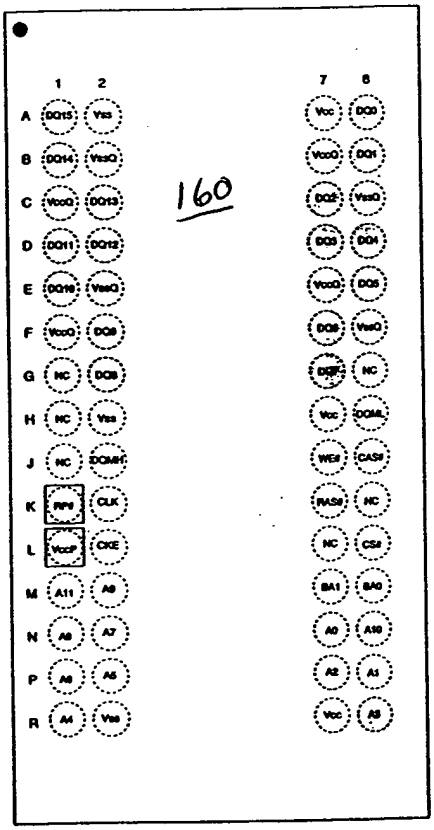

1 2
7 8
A DQ15 Vss Vcc DQ0
B DQ14 VssQ VccQ DQ1
C VccQ DQ13 DQ2 VssQ
D DQ11 DQ12 DQ3 DQ4
E DQ10 VssQ VccQ DQ5
F VccQ DQ9 DQ6 VssQ
G NC DQ8 DQF7 NC
H NC Vss Vcc DQML
J NC DQMH WE# CAS#
K RP# CLK RAS# NC
L VccP CKE NC CS#
M A11 A9 BA1 BA0
N A8 A7 A0 A10
P A6 A5 A2 A1
R A4 Vss Vcc A3
160

Fig. 1C

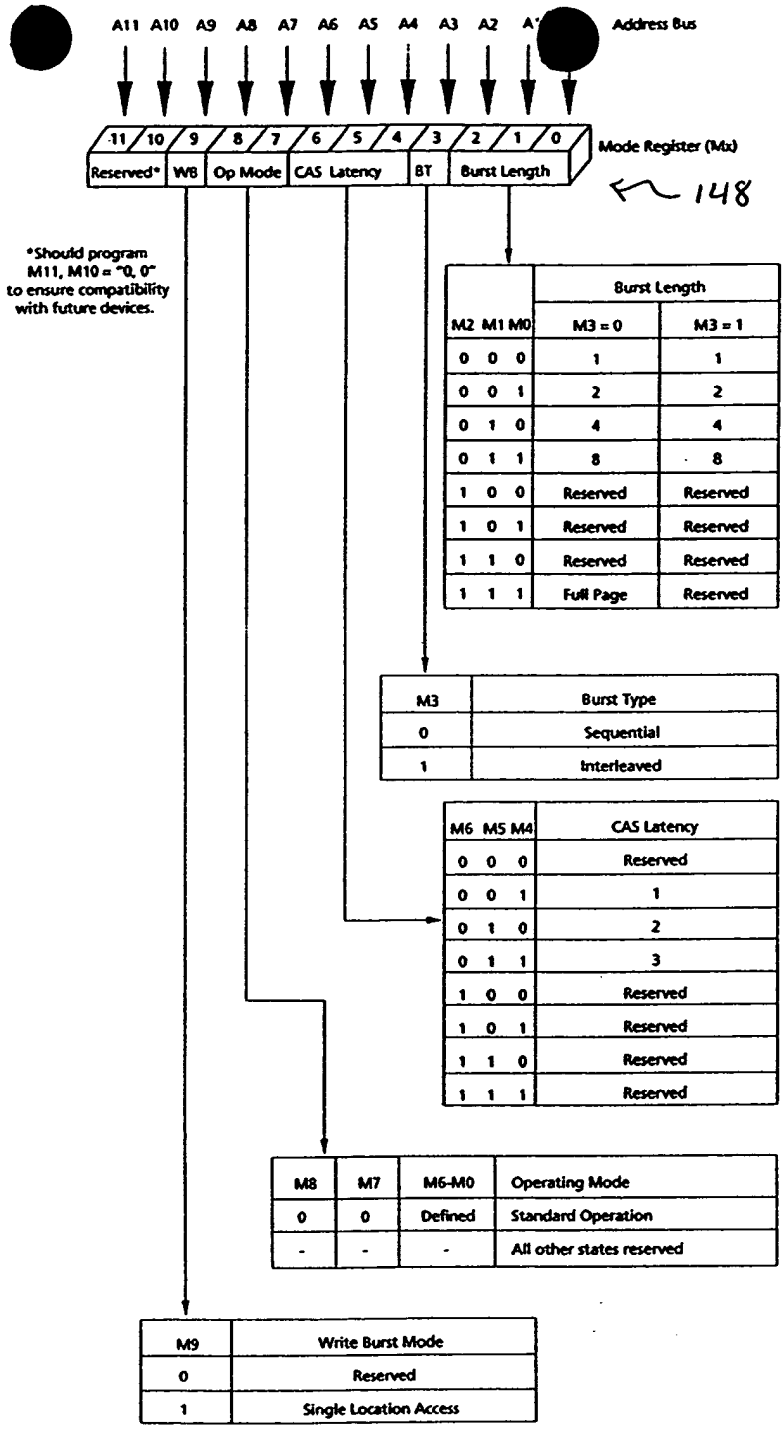

A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
Address Bus
11 10 9 8 7 6 5 4 3 2 1 0
Reserved* WB Op Mode CAS Latency BT Burst Length
Mode Register (Mx)
148
*Should program M11, M10 = "0, 0" to ensure compatibility with future devices.
Burst Length
M2 M1 M0 | M3 = 0 | M3 = 1
0 0 0 | 1 | 1
0 0 1 | 2 | 2
0 1 0 | 4 | 4
0 1 1 | 8 | 8
1 0 0 | Reserved | Reserved
1 0 1 | Reserved | Reserved
1 1 0 | Reserved | Reserved
1 1 1 | Full Page | Reserved
M3 | Burst Type
0 | Sequential
1 | Interleaved
M6 M5 M4 | CAS Latency
0 0 0 | Reserved
0 0 1 | 1
0 1 0 | 2
0 1 1 | 3
1 0 0 | Reserved
1 0 1 | Reserved
1 1 0 | Reserved
1 1 1 | Reserved
M8 | M7 | M6-M0 | Operating Mode
0 | 0 | Defined | Standard Operation
- | - | - | All other states reserved
M9 | Write Burst Mode
0 | Reserved
1 | Single Location Access

Fig. 2

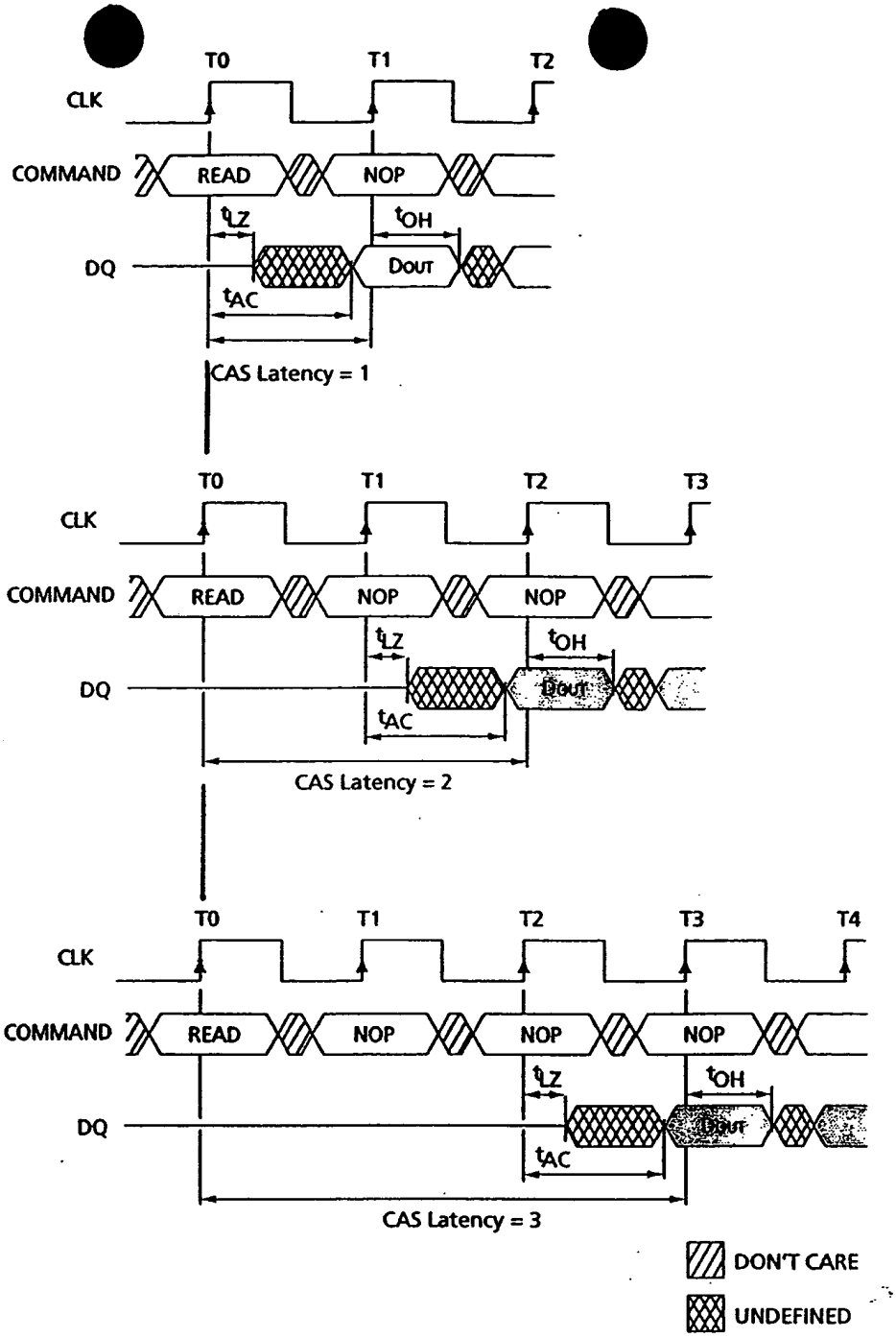

T0
T1
T2
CLK
COMMAND
READ
NOP
tLZ
tOH
DQ
DOUT
tAC
CAS Latency = 1
T0
T1
T2
T3
CLK
COMMAND
READ
NOP
NOP
tLZ
tOH
DQ
DOUT
tAC
CAS Latency = 2
T0
T1
T2
T3
T4
CLK
COMMAND
READ
NOP
NOP
NOP
tLZ
tOH
DQ
DOUT
tAC
CAS Latency = 3
DON'T CARE
UNDEFINED

Fig. 3

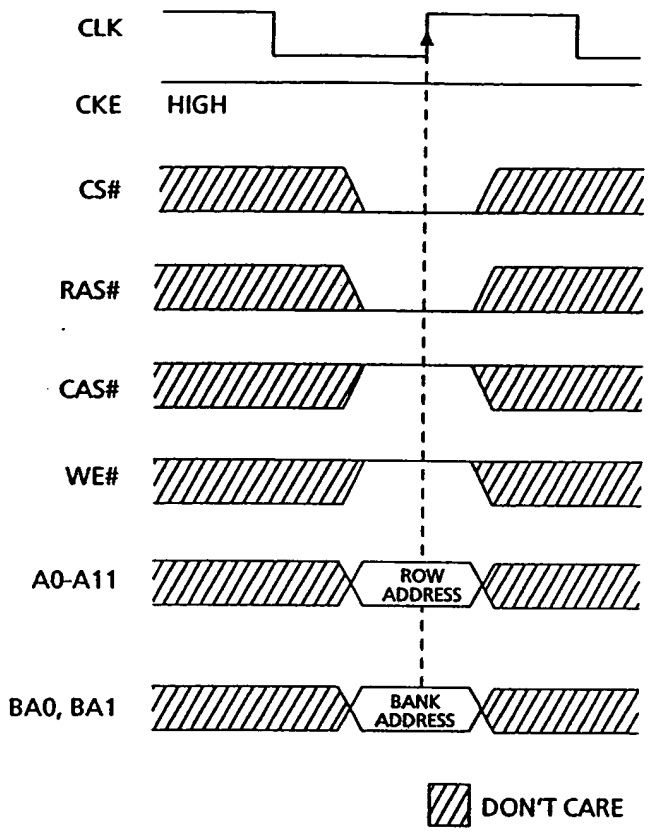

CLK
CKE
HIGH
CS#
RAS#
CAS#
WE#
A0-A11
ROW ADDRESS
BA0, BA1
BANK ADDRESS
DON'T CARE

Fig. 4

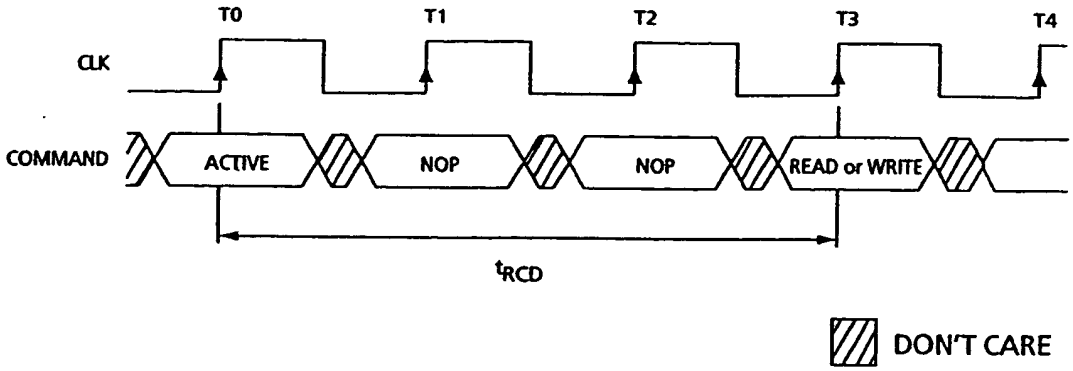

T0
T1
T2
T3
T4
CLK
COMMAND
ACTIVE
NOP
NOP
READ or WRITE
tRCD
DON'T CARE

Fig. 5

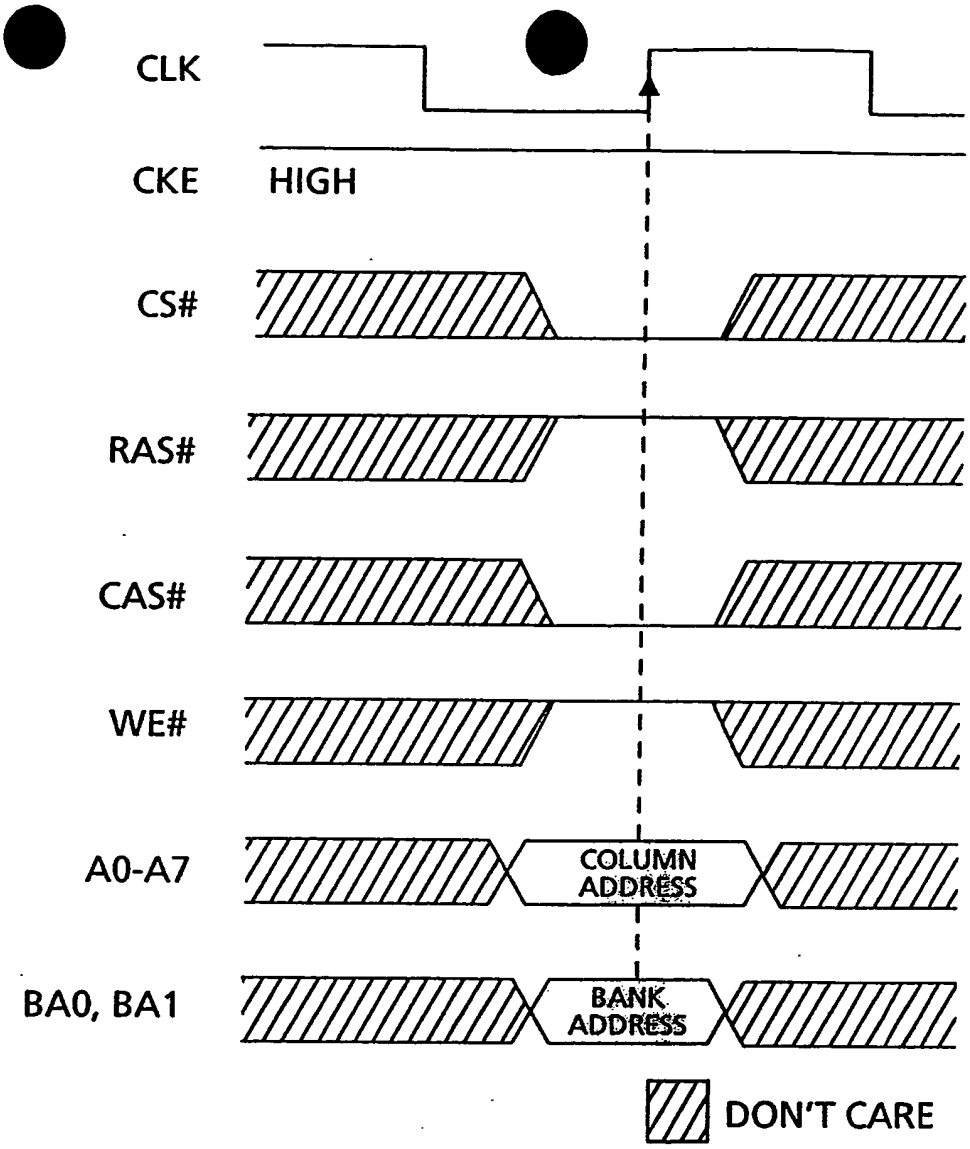
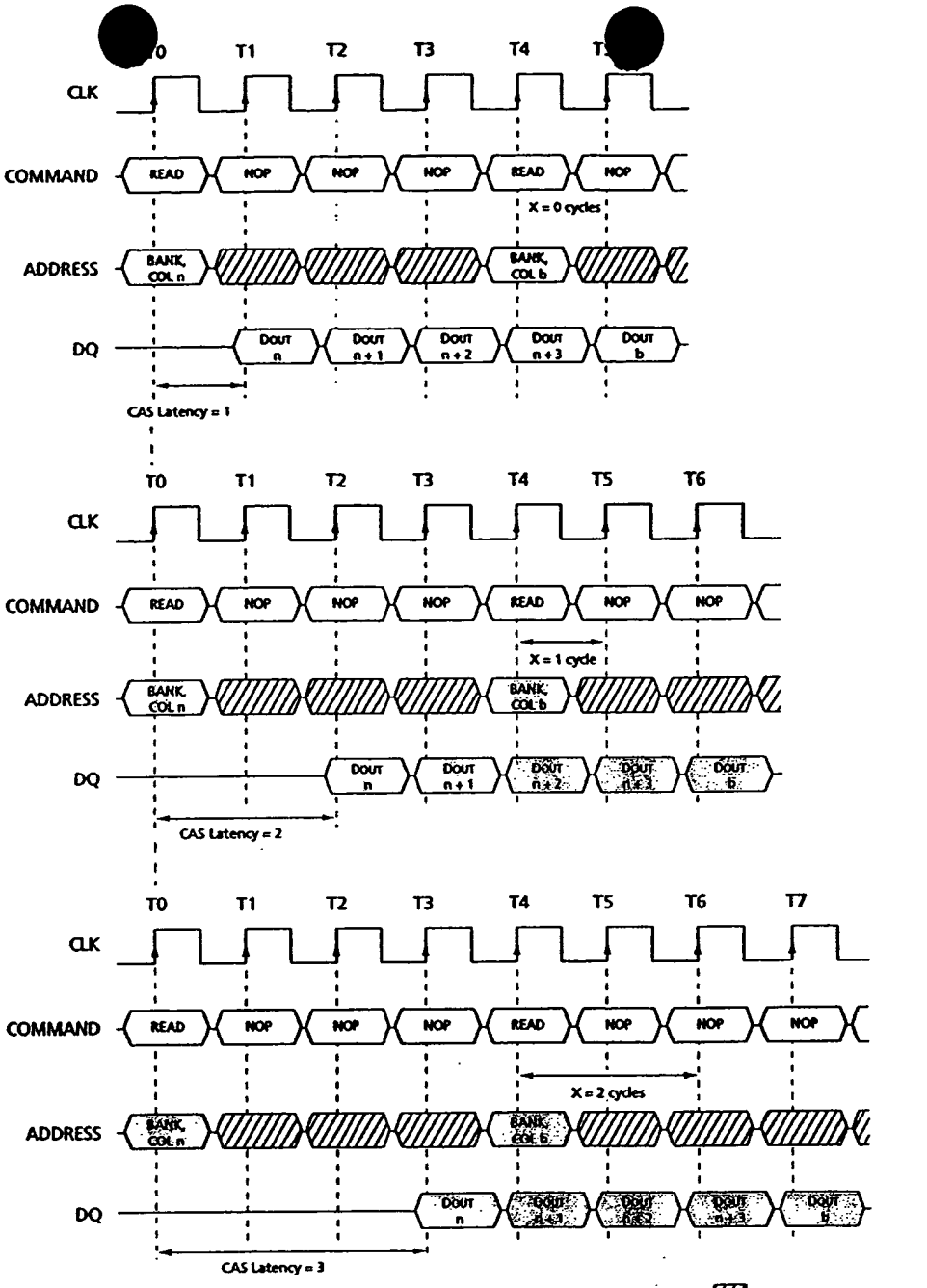
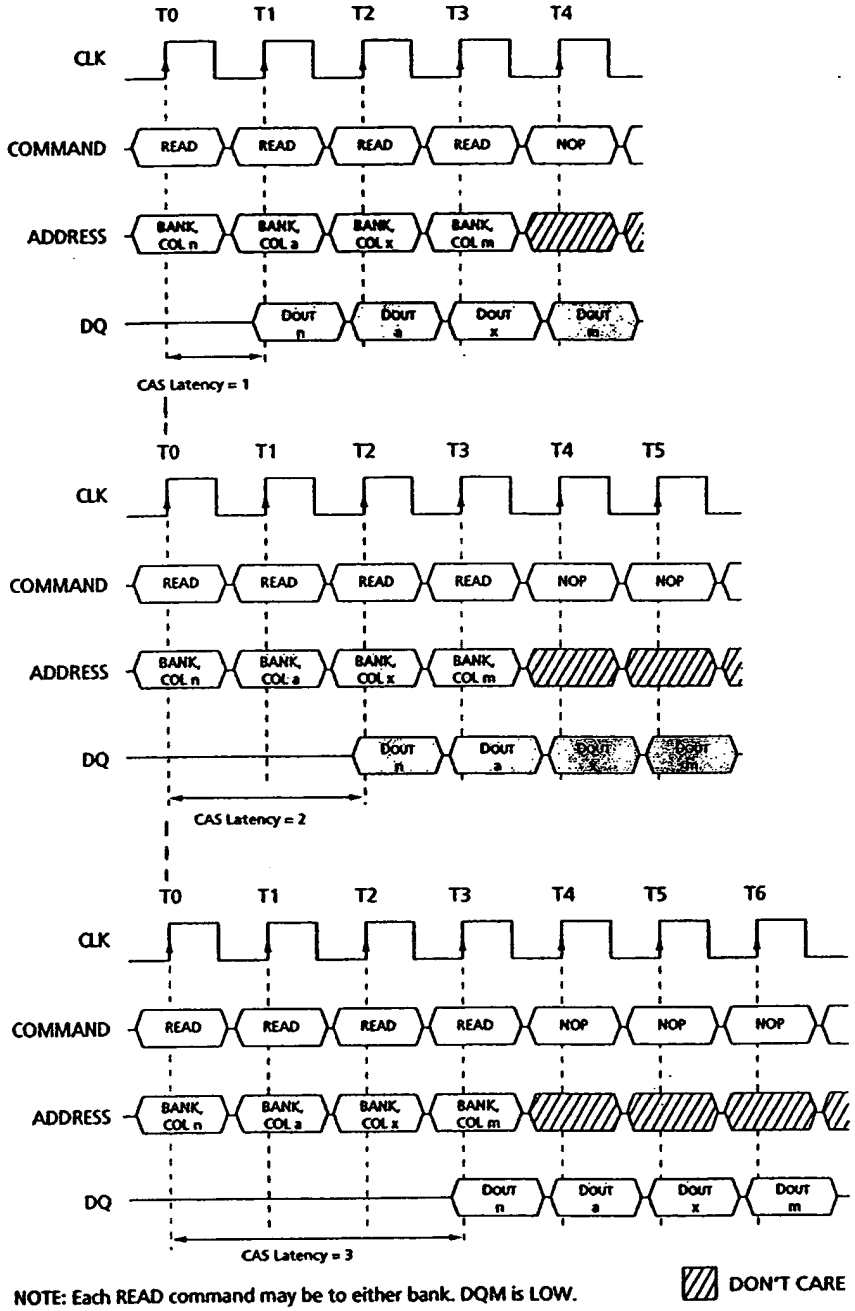

CLK
CKE
HIGH
CS#
RAS#
CAS#
WE#
A0-A7
COLUMN ADDRESS
BA0, BA1
BANK ADDRESS
DON'T CARE

Fig. 6



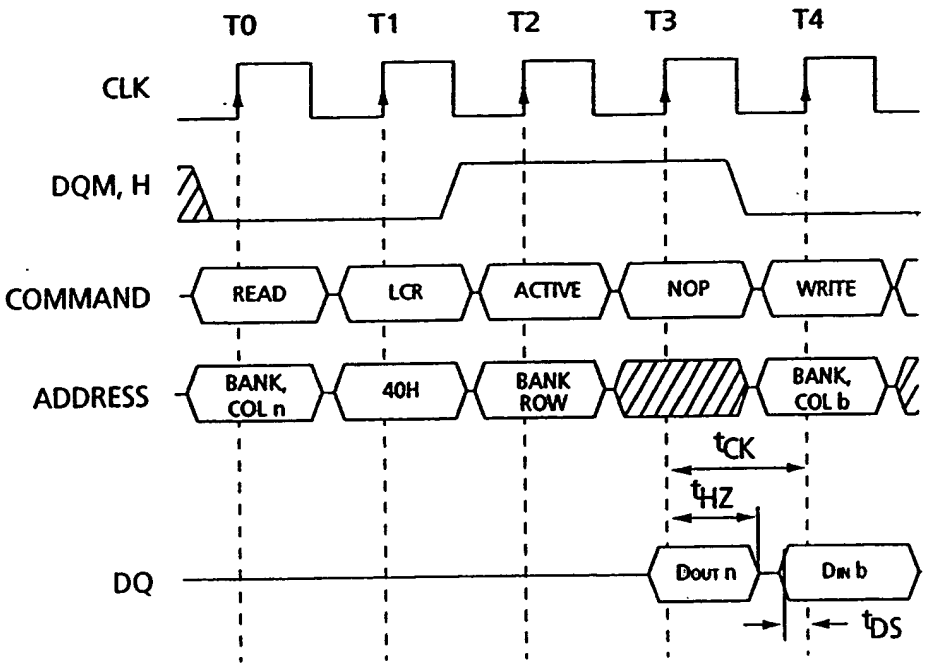
NOTE: Each READ command may be to either bank. DQM is LOW.

Fig. 7



NOTE: Each READ command may be to either bank. DQM is LOW.

Fig. 8



NOTE: A CAS latency of three is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank. If a CAS latency of one is used, then DQM is not required.

DON'T CARE

Fig 9

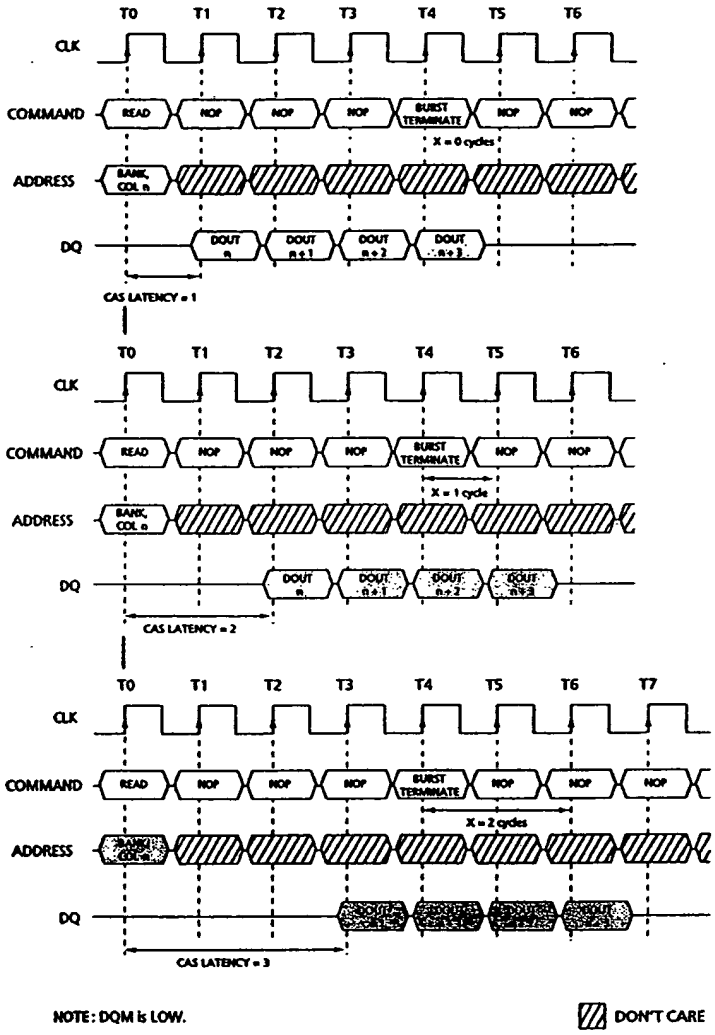

T0
T1
T2
T3
T4
T5
T6
T7
CLK
COMMAND
READ
NOP
BURST TERMINATE
X = 0 cycles
ADDRESS
BANK, COL n
DQ
DOUT n
DOUT n+1
DOUT n+2
DOUT n+3
CAS LATENCY = 1
X = 1 cycle
CAS LATENCY = 2
X = 2 cycles
CAS LATENCY = 3
NOTE: DQM is LOW.
DON'T CARE

Fig. 10

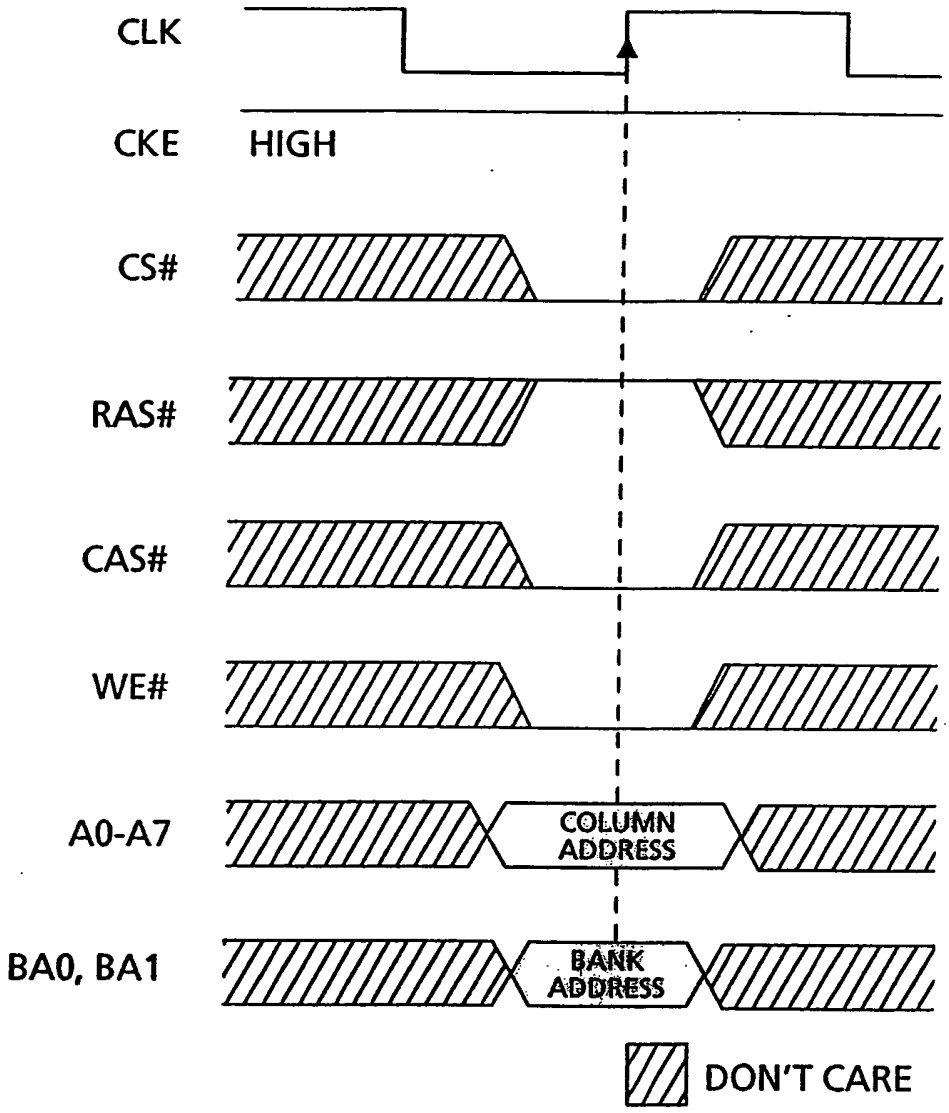
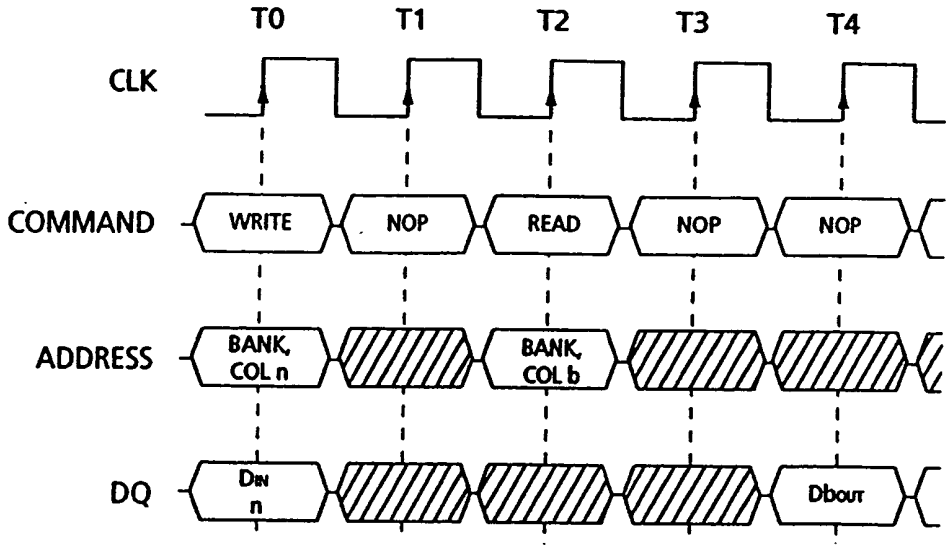

CLK
CKE
HIGH
CS#
RAS#
CAS#
WE#
A0-A7
COLUMN ADDRESS
BA0, BA1
BANK ADDRESS
DON'T CARE

Fig. 11



NOTE: A CAS latency of two is used for illustration. The WRITE command may be to any bank and the READ command may be to any bank. DQM is LOW. A READ to the bank undergoing the WRITE ISM operation may output invalid data. Tables 4 and 5.

▨ DON'T CARE

Fig. 12

Coming out of a power-down sequence (active),
^{t}CKS (CKE setup time) must be greater than or equal to 3ns.

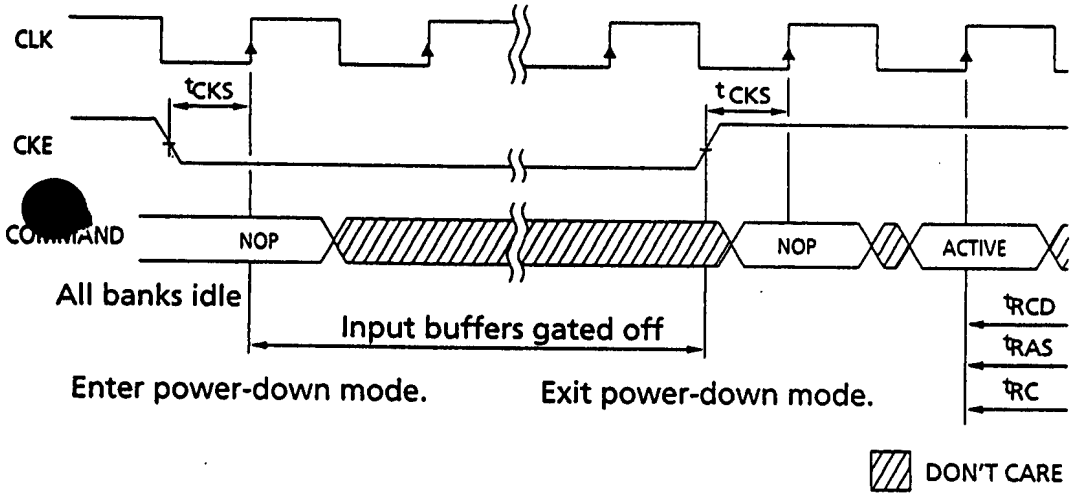
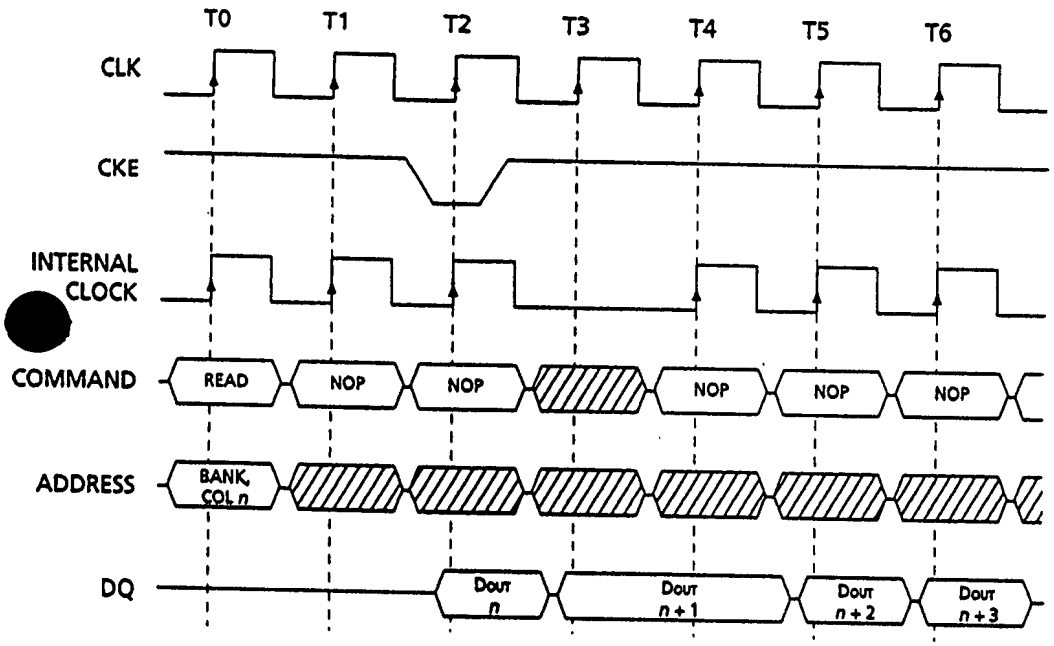


Fig. 13



NOTE: For this example, CAS latency = 2, burst length = 4 or greater, an DQM is LOW.

▨ DON'T CARE

Fig. 14

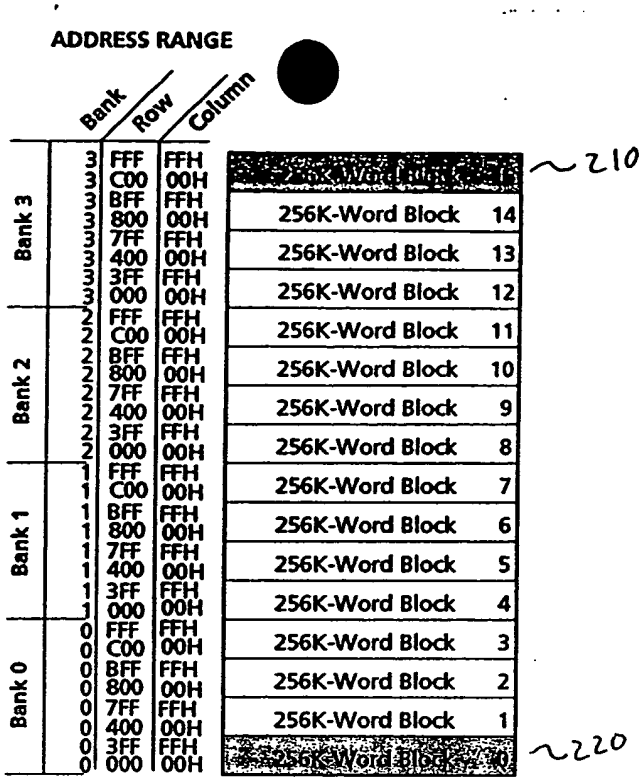

ADDRESS RANGE
Bank
Row
Column
Bank 3
Bank 2
Bank 1
Bank 0
3 FFF FFH
3 C00 00H
3 BFF FFH
3 800 00H
3 7FF FFH
3 400 00H
3 3FF FFH
3 000 00H
2 FFF FFH
2 C00 00H
2 BFF FFH
2 800 00H
2 7FF FFH
2 400 00H
2 3FF FFH
2 000 00H
1 FFF FFH
1 C00 00H
1 BFF FFH
1 800 00H
1 7FF FFH
1 400 00H
1 3FF FFH
1 000 00H
0 FFF FFH
0 C00 00H
0 BFF FFH
0 800 00H
0 7FF FFH
0 400 00H
0 3FF FFH
0 000 00H
256K-Word Block 15
256K-Word Block 14
256K-Word Block 13
256K-Word Block 12
256K-Word Block 11
256K-Word Block 10
256K-Word Block 9
256K-Word Block 8
256K-Word Block 7
256K-Word Block 6
256K-Word Block 5
256K-Word Block 4
256K-Word Block 3
256K-Word Block 2
256K-Word Block 1
256K-Word Block 0
~210
~220
Word-wide (x16)
Software Lock = Hardware-Lock Sectors
RP# = VHH to unprotect if either the block protect or device protect bit is set.
Software Lock = Hardware-Lock Sectors
RP# = VCC to unprotect but must be VHH if the device protect bit is set.
See BLOCK PROTECT/UNPROTECT SEQUENCE for detailed information.

Fig. 15

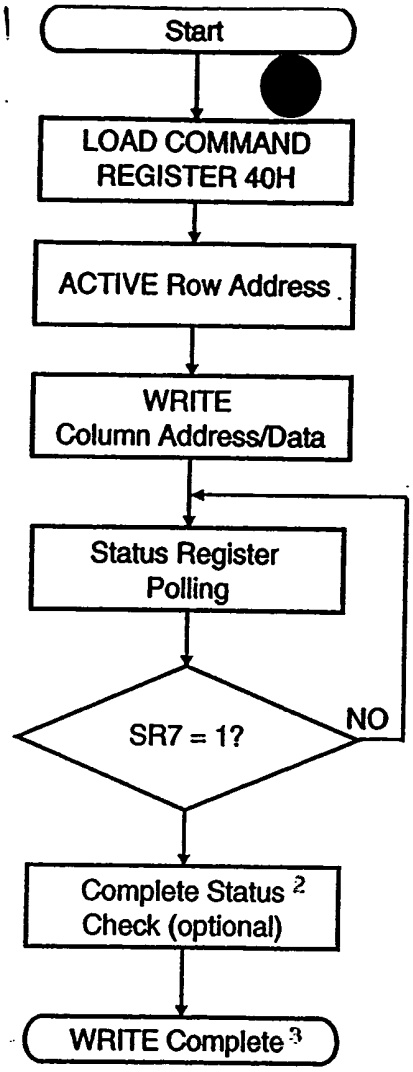

Start
LOAD COMMAND REGISTER 40H
ACTIVE Row Address
WRITE Column Address/Data
Status Register Polling
SR7 = 1?
NO
Complete Status Check (optional) 2
WRITE Complete 3

Fig. 16

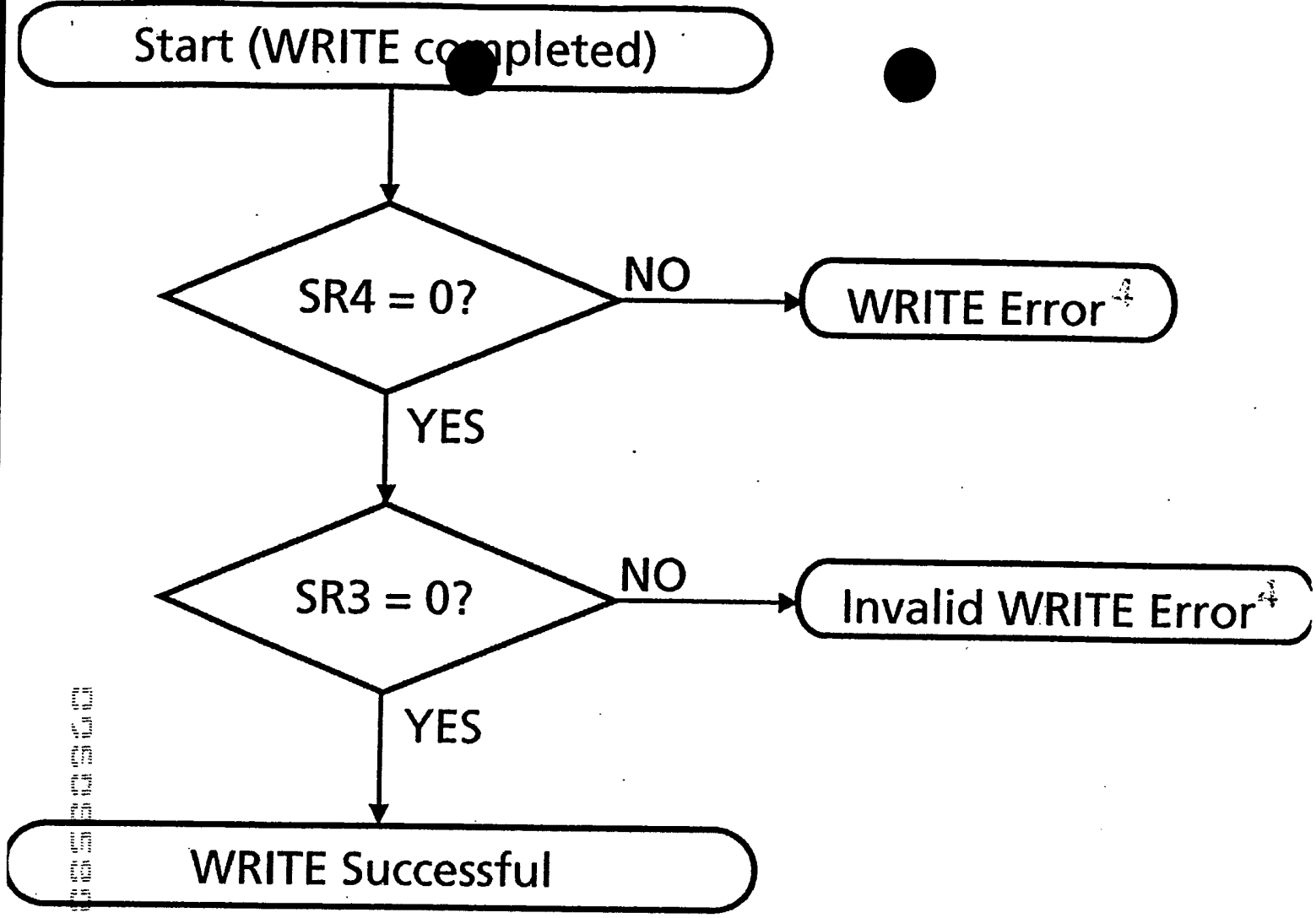

Start (WRITE completed)
SR4 = 0?
NO
WRITE Error
YES
SR3 = 0?
NO
Invalid WRITE Error
YES
WRITE Successful

Fig. 17

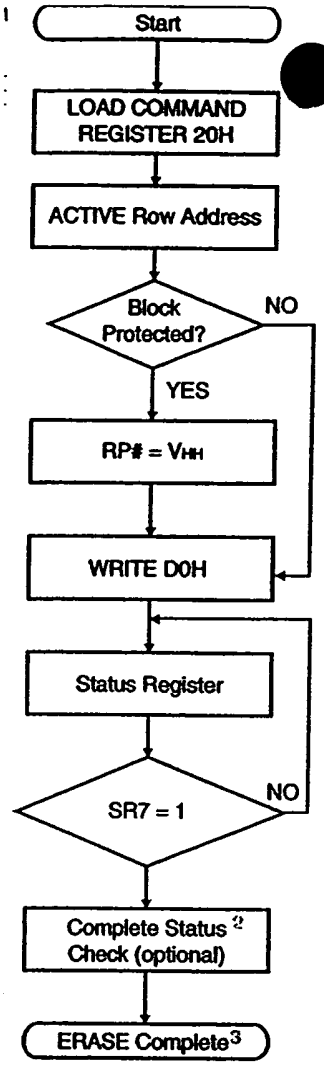

Start
LOAD COMMAND REGISTER 20H
ACTIVE Row Address
Block Protected?
NO
YES
RP# = VHH
WRITE D0H
Status Register
SR7 = 1
NO
Complete Status Check (optional) 2
ERASE Complete 3

Fig. 18

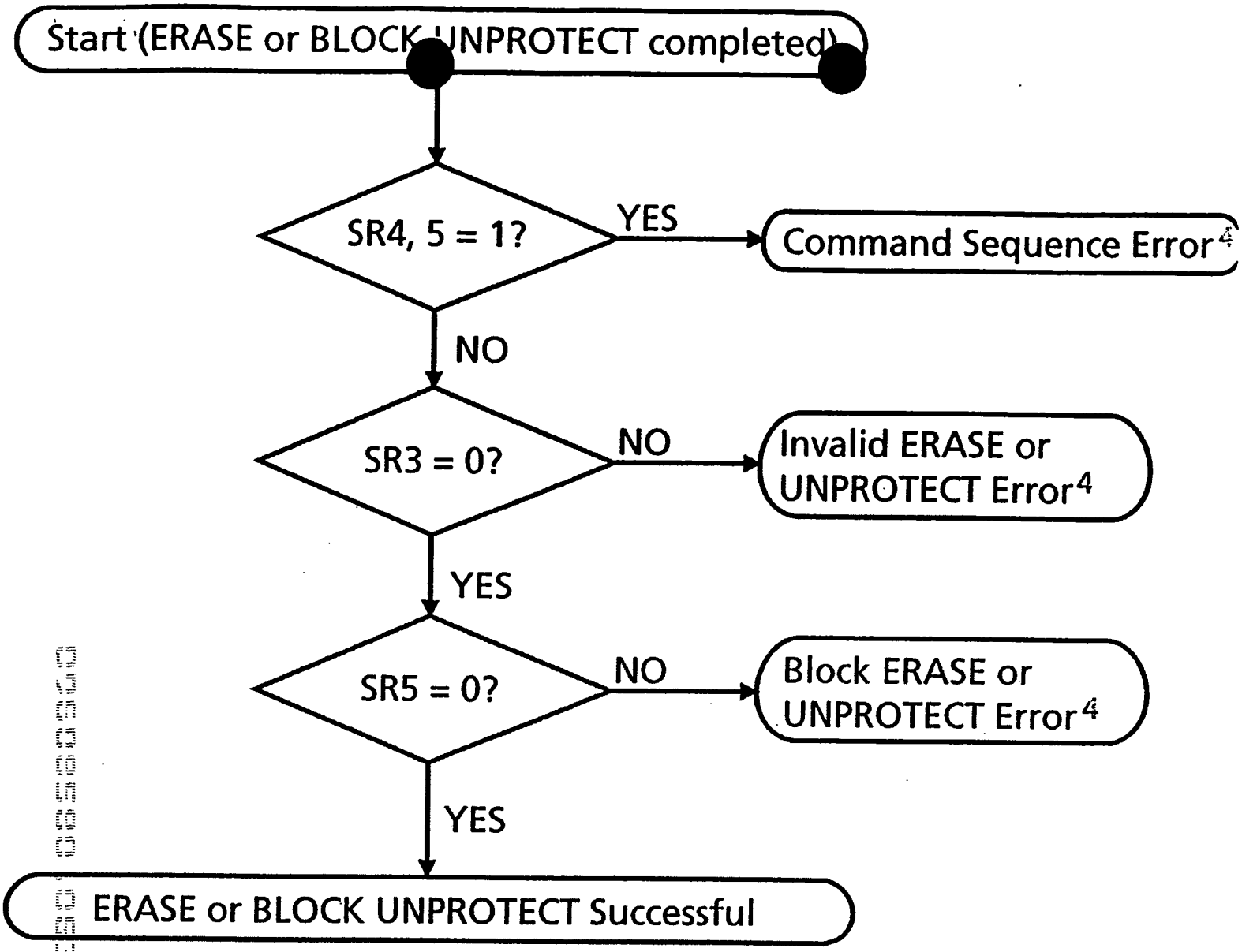

Start (ERASE or BLOCK UNPROTECT completed)
SR4, 5 = 1?
YES
Command Sequence Error[4]
NO
SR3 = 0?
NO
Invalid ERASE or UNPROTECT Error[4]
YES
SR5 = 0?
NO
Block ERASE or UNPROTECT Error[4]
YES
ERASE or BLOCK UNPROTECT Successful

Fig. 19

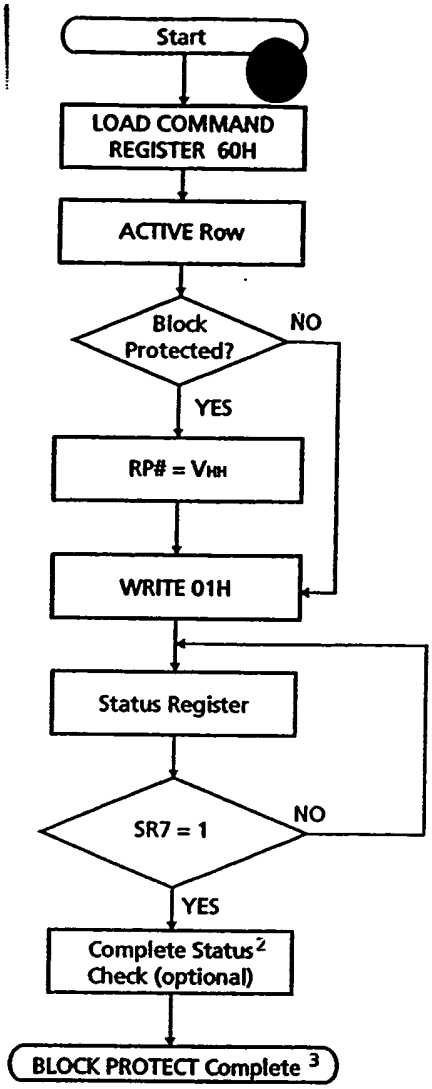

Start
LOAD COMMAND REGISTER 60H
ACTIVE Row
Block Protected?
NO
YES
RP# = VHH
WRITE 01H
Status Register
SR7 = 1
NO
YES
Complete Status Check (optional) 2
BLOCK PROTECT Complete 3

Fig. 20

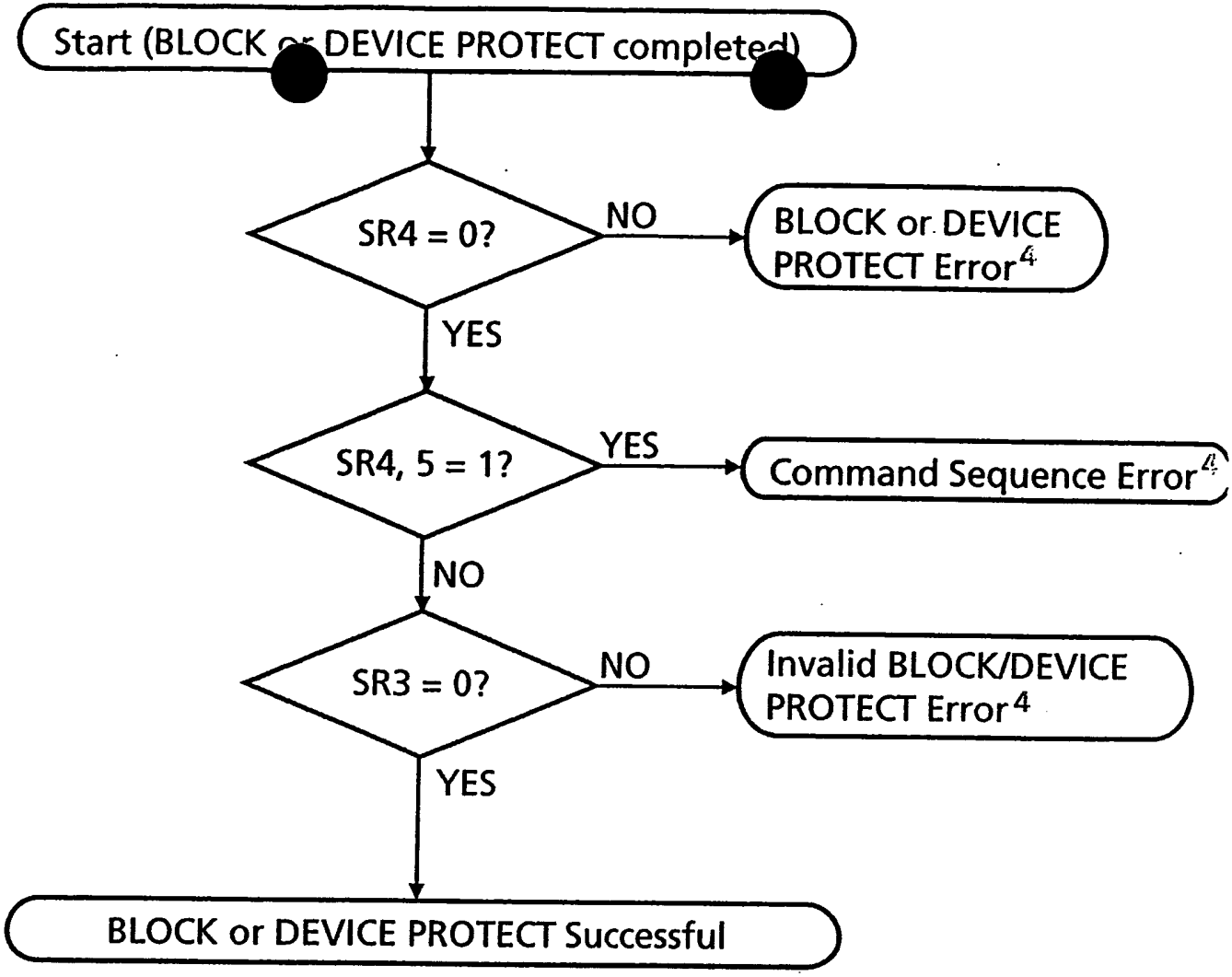

Start (BLOCK or DEVICE PROTECT completed)
SR4 = 0?
NO
BLOCK or DEVICE PROTECT Error[4]
YES
SR4, 5 = 1?
YES
Command Sequence Error[4]
NO
SR3 = 0?
NO
Invalid BLOCK/DEVICE PROTECT Error[4]
YES
BLOCK or DEVICE PROTECT Successful

Fig. 21

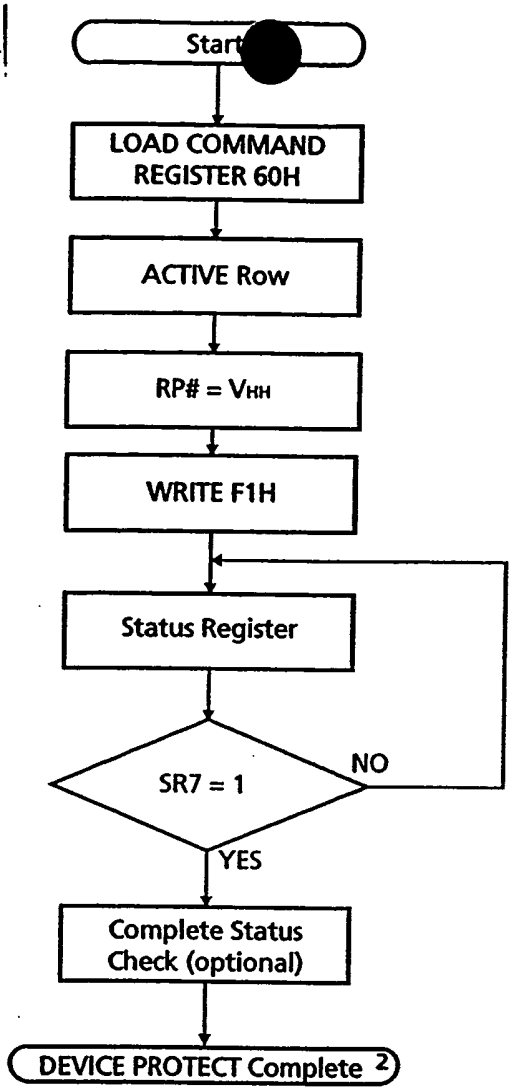

Start
LOAD COMMAND REGISTER 60H
ACTIVE Row
RP# = VHH
WRITE F1H
Status Register
SR7 = 1
NO
YES
Complete Status Check (optional)
DEVICE PROTECT Complete 2

Fig. 22

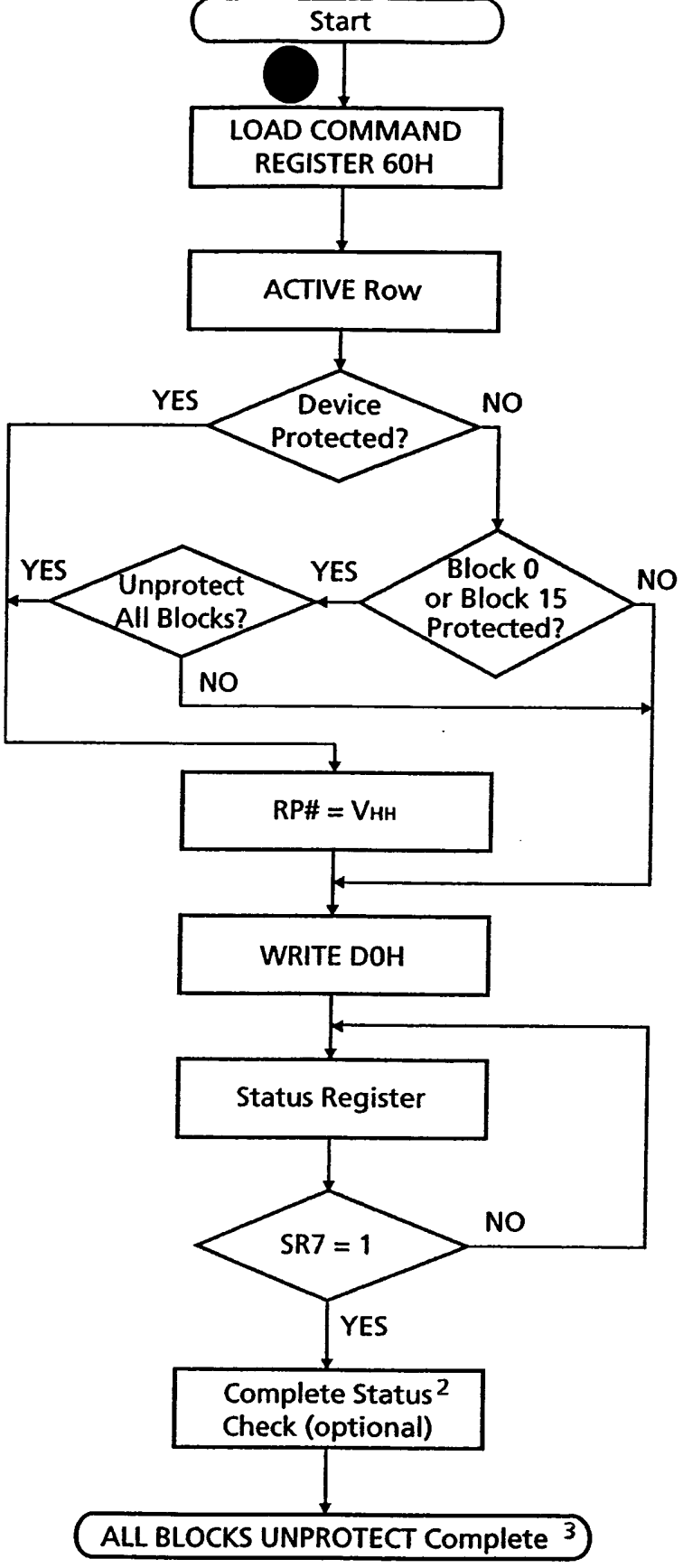

Start
LOAD COMMAND REGISTER 60H
ACTIVE Row
Device Protected?
YES
NO
Block 0 or Block 15 Protected?
YES
NO
Unprotect All Blocks?
YES
NO
RP# = VHH
WRITE D0H
Status Register
SR7 = 1
NO
YES
Complete Status Check (optional) 2
ALL BLOCKS UNPROTECT Complete 3

Fig. 23

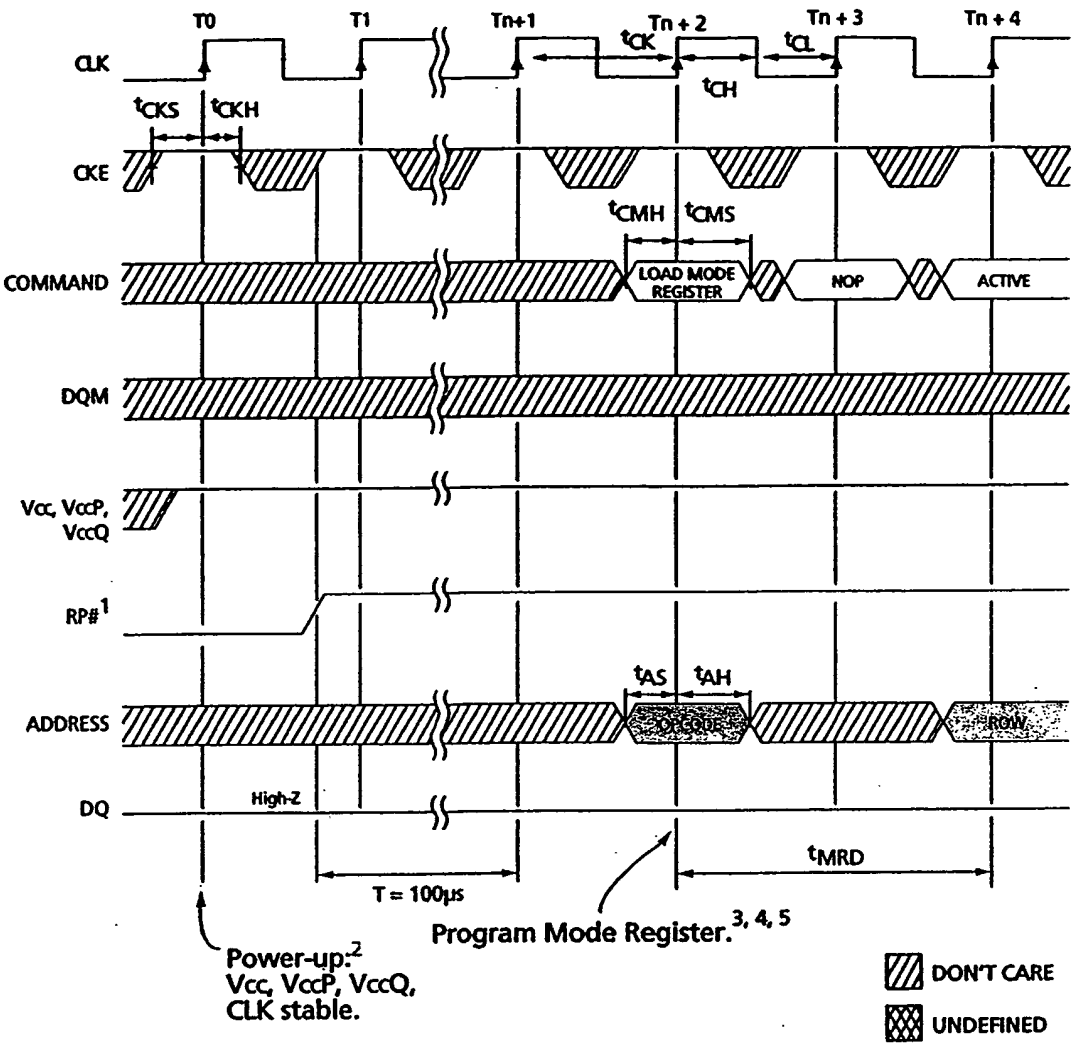

T0
T1
Tn+1
Tn + 2
Tn + 3
Tn + 4
CLK
tCK
tCL
tCH
tCKS
tCKH
CKE
tCMH
tCMS
COMMAND
LOAD MODE REGISTER
NOP
ACTIVE
DQM
Vcc, VccP, VccQ
RP#1
tAS
tAH
ADDRESS
OP CODE
ROW
DQ
High-Z
tMRD
T = 100µs
Program Mode Register.3, 4, 5
Power-up:2
Vcc, VccP, VccQ,
CLK stable.
DON'T CARE
UNDEFINED

Fig. 24

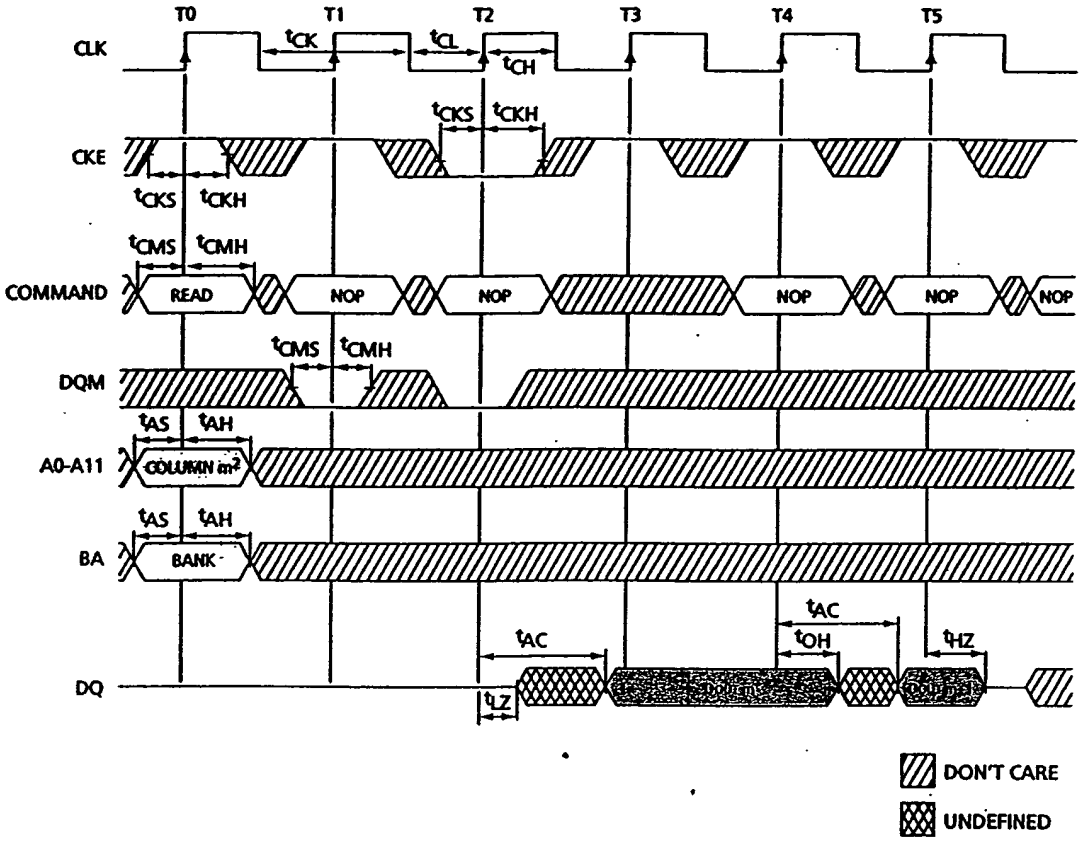

T0
T1
T2
T3
T4
T5
CLK
tCK
tCL
tCH
CKE
tCKS
tCKH
COMMAND
tCMS
tCMH
READ
NOP
DQM
tAS
tAH
A0-A11
COLUMN m
BA
BANK
tAC
tOH
tHZ
tLZ
DQ
DON'T CARE
UNDEFINED

Fig. 25

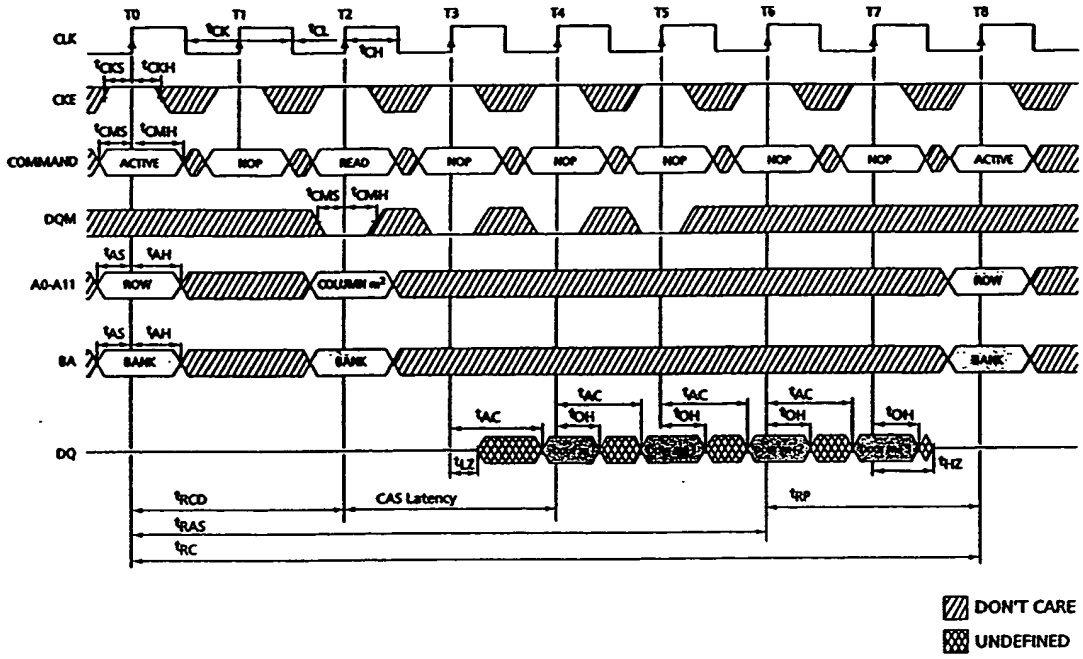

T0
T1
T2
T3
T4
T5
T6
T7
T8
CLK
CKE
COMMAND
ACTIVE
NOP
READ
NOP
NOP
NOP
NOP
NOP
ACTIVE
DQM
A0-A11
ROW
COLUMN m
ROW
BA
BANK
BANK
BANK
DQ
CAS Latency
DON'T CARE
UNDEFINED

Fig. 26

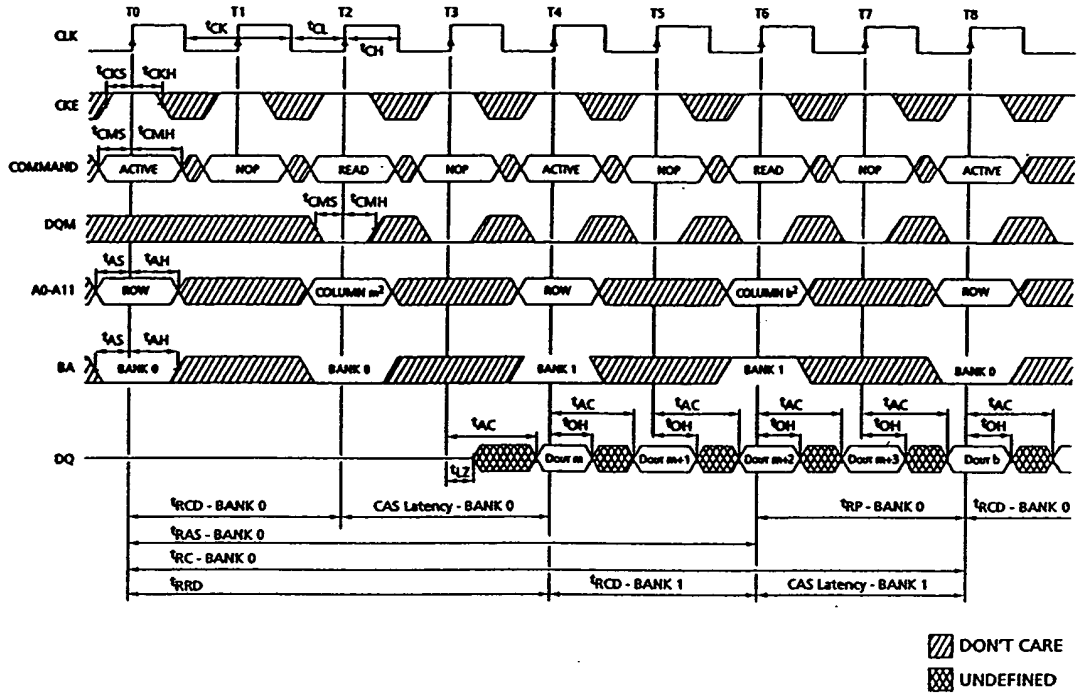

T0
T1
T2
T3
T4
T5
T6
T7
T8
CLK
CKE
COMMAND
DQM
A0-A11
BA
DQ
ACTIVE
NOP
READ
ROW
BANK 0
BANK 1
tRCD - BANK 0
CAS Latency - BANK 0
tRP - BANK 0
tRAS - BANK 0
tRC - BANK 0
tRRD
tRCD - BANK 1
CAS Latency - BANK 1
DON'T CARE
UNDEFINED

Fig. 27

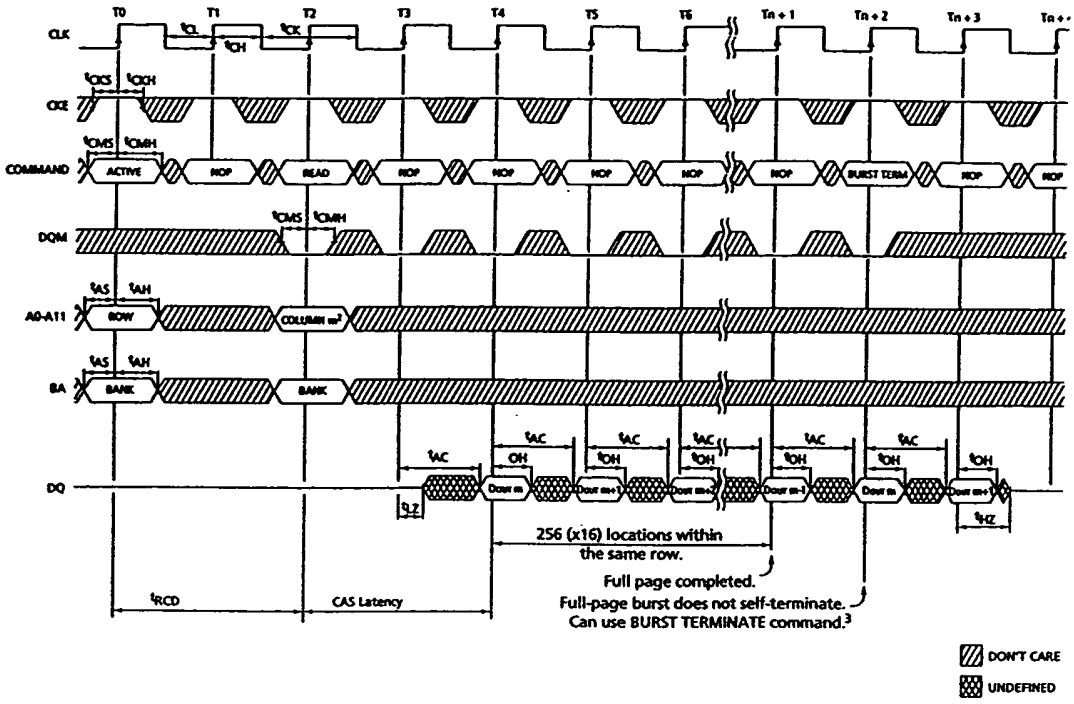
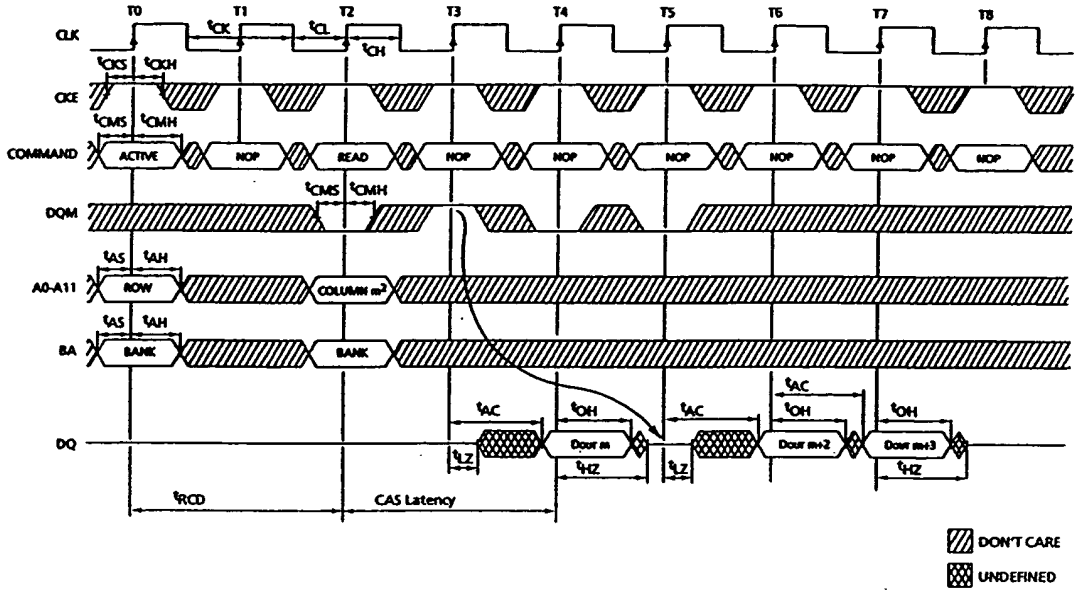

T0
T1
T2
T3
T4
T5
T6
Tn + 1
Tn + 2
Tn + 3
CLK
CKE
COMMAND
ACTIVE
NOP
READ
BURST TERM
DQM
A0-A11
ROW
COLUMN m²
BA
BANK
DQ
Dout m
Dout m+1
Dout m+2
Dout m+3
256 (x16) locations within the same row.
Full page completed.
Full-page burst does not self-terminate.
Can use BURST TERMINATE command.³
CAS Latency
DON'T CARE
UNDEFINED

Fig. 28


T0
T1
T2
T3
T4
T5
T6
T7
T8
CLK
tCK
tCL
tCH
tCKS
tCKH
CKE
tCMS
tCMH
COMMAND
ACTIVE
NOP
READ
NOP
NOP
NOP
NOP
NOP
NOP
tCMS
tCMH
DQM
tAS
tAH
A0-A11
ROW
COLUMN m
tAS
tAH
BA
BANK
BANK
tAC
tOH
tAC
tAC
tOH
tOH
DQ
tLZ
Dout m
tHZ
tLZ
Dout m+2
Dout m+3
tHZ
tRCD
CAS Latency
DON'T CARE
UNDEFINED

Frg. 29

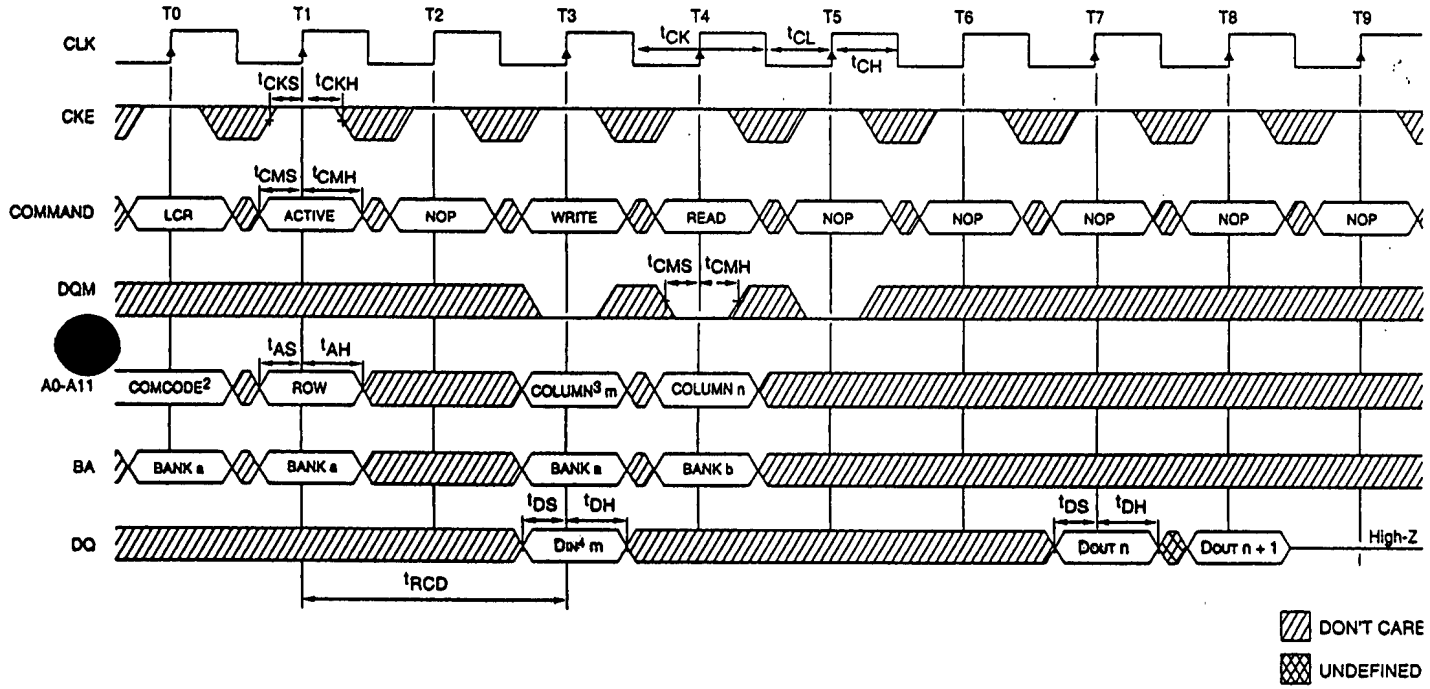

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
CLK
CKE
COMMAND
DQM
A0-A11
BA
DQ
tCK
tCL
tCH
tCKS
tCKH
tCMS
tCMH
tAS
tAH
tDS
tDH
tRCD
LCR
ACTIVE
NOP
WRITE
READ
COMCODE2
ROW
COLUMN3 m
COLUMN n
BANK a
BANK b
DOUT n
DOUT n + 1
High-Z
DON'T CARE
UNDEFINED

Fig. 30

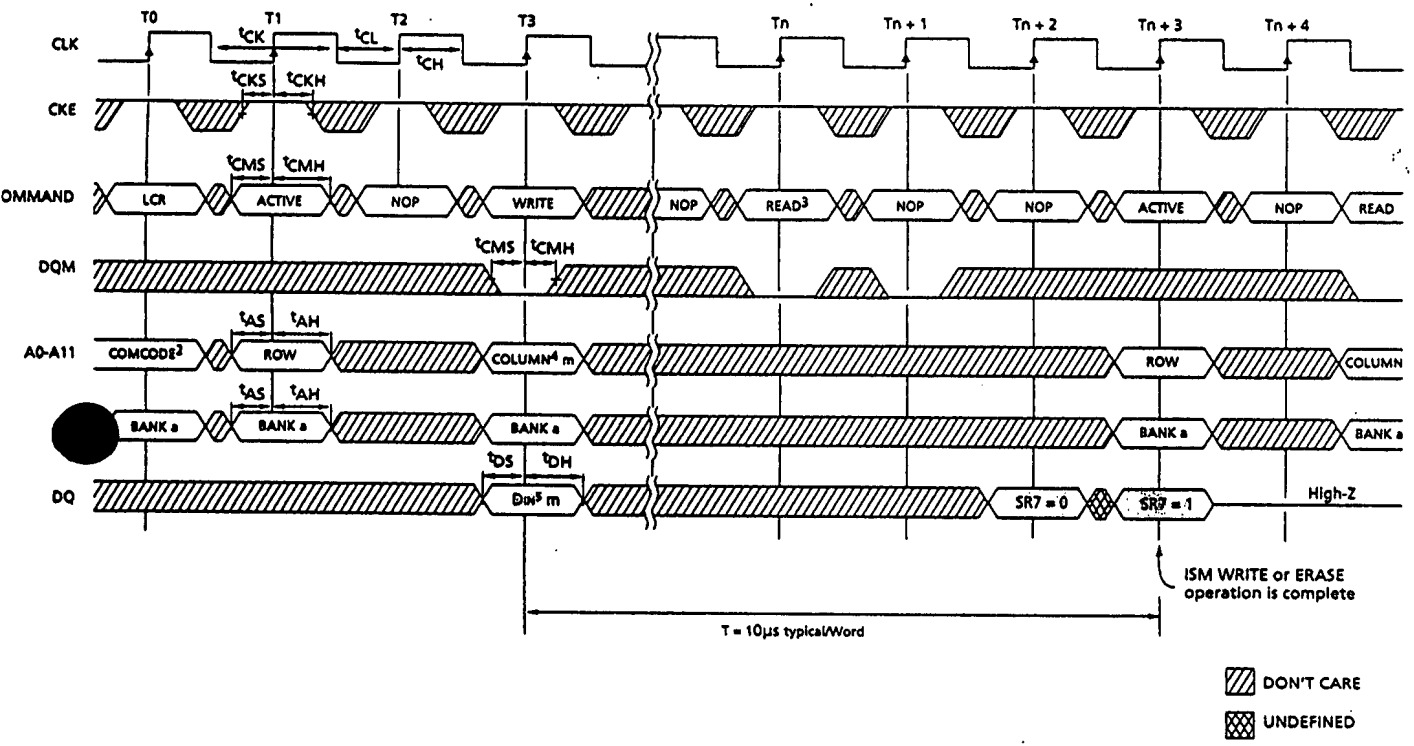

T0
T1
T2
T3
Tn
Tn + 1
Tn + 2
Tn + 3
Tn + 4
CLK
CKE
COMMAND
DQM
A0-A11
DQ
LCR
ACTIVE
NOP
WRITE
READ3
ACTIVE
READ
COMCODE2
ROW
COLUMN4 m
BANK a
DIN5 m
SR7 = 0
SR7 = 1
High-Z
ISM WRITE or ERASE operation is complete
T = 10µs typical/Word
DON'T CARE
UNDEFINED

Fig. 31

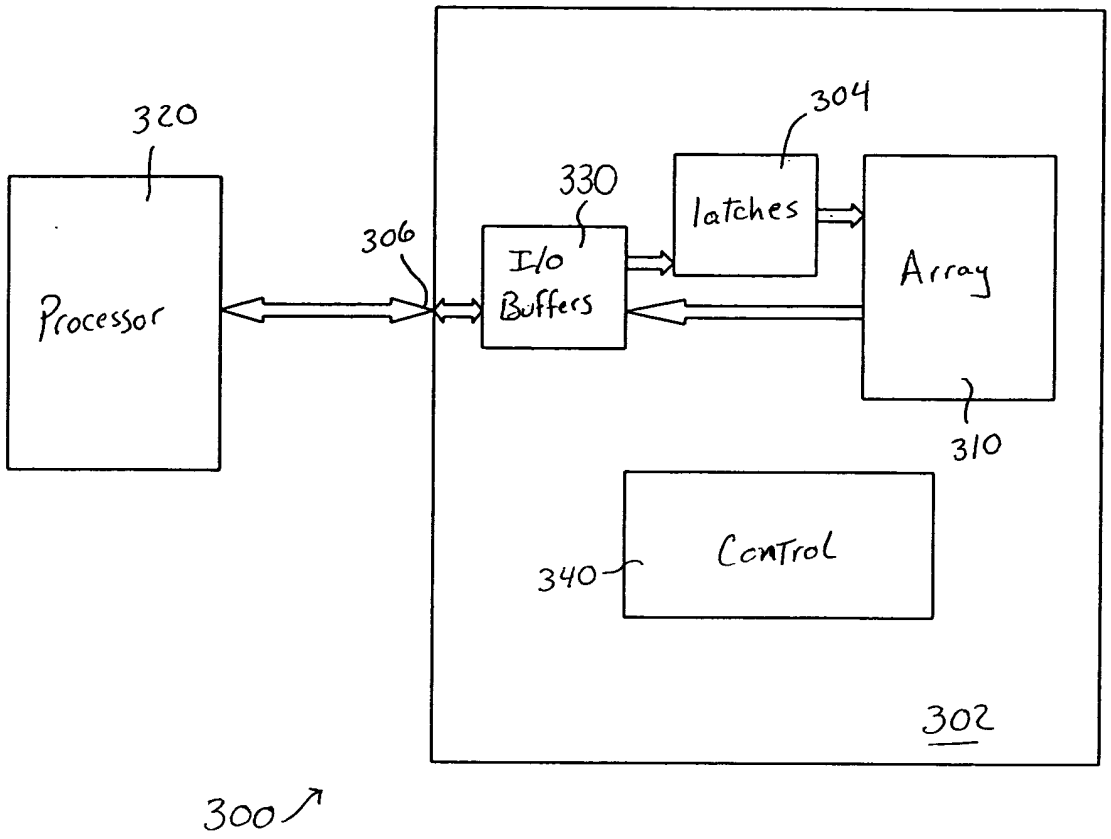

320
Processor
306
330
I/o
Buffers
304
latches
Array
310
340
Control
302
300

Fig. 32